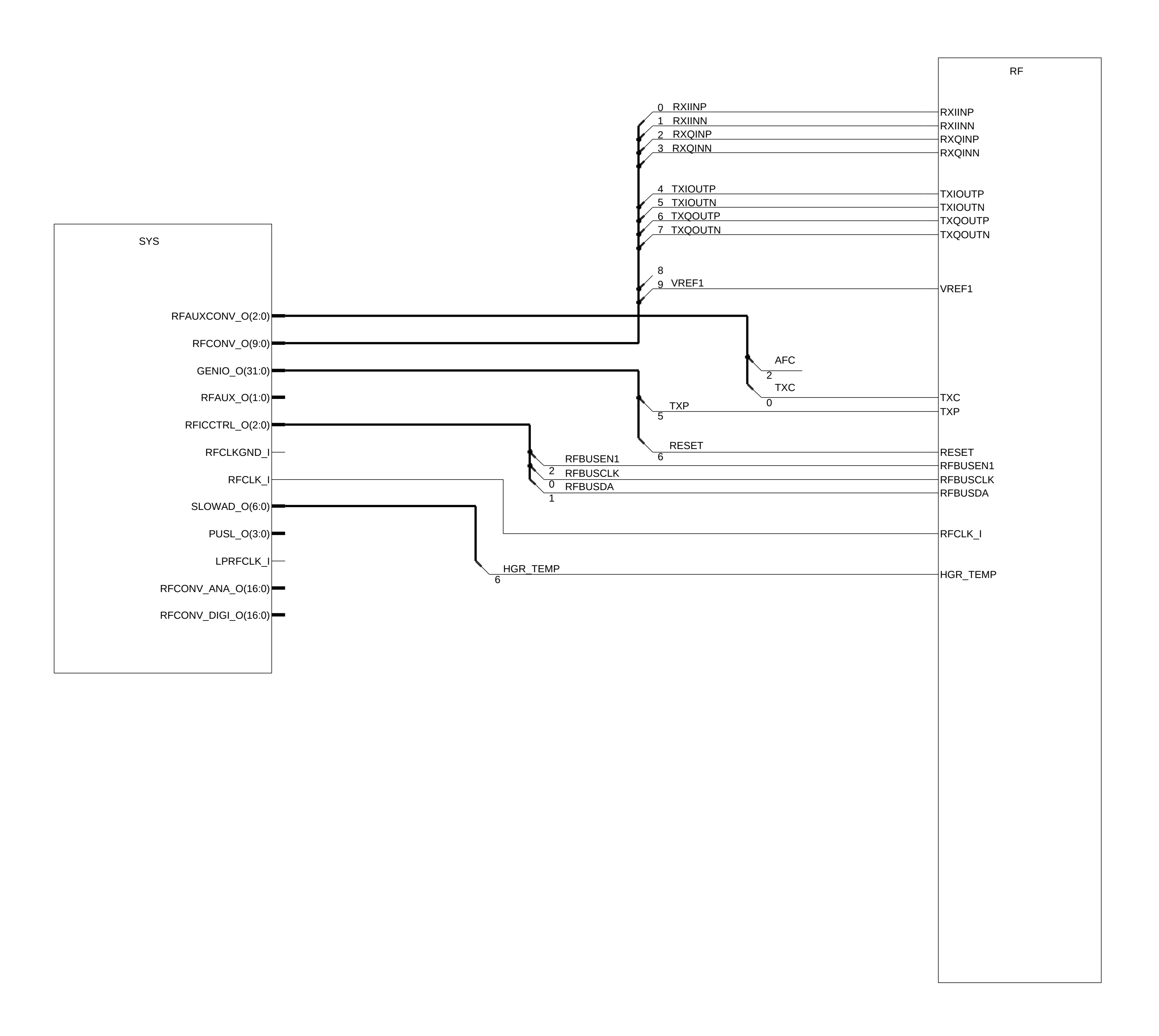
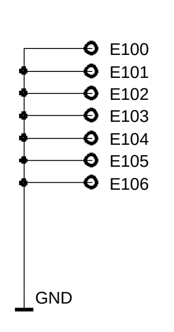
10 - SCHEMATICS

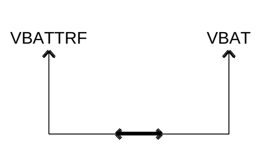
Table of Contents

Title: Top level schematic

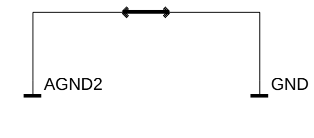


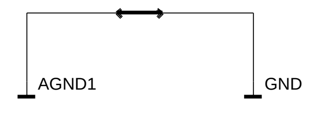
Title: Top sheet (2)

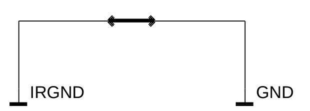




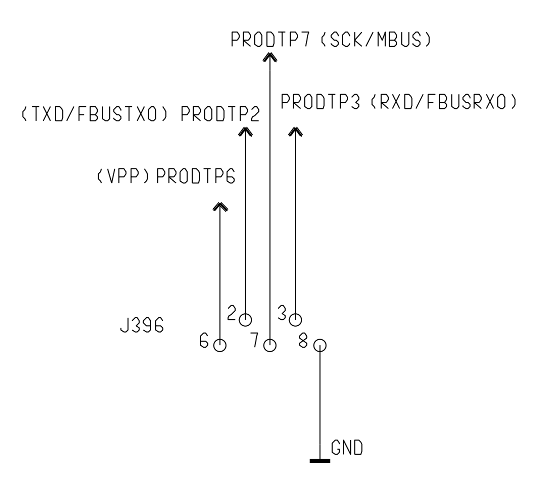
Title: DCT4 Common Baseband Schematic (Top level 2)



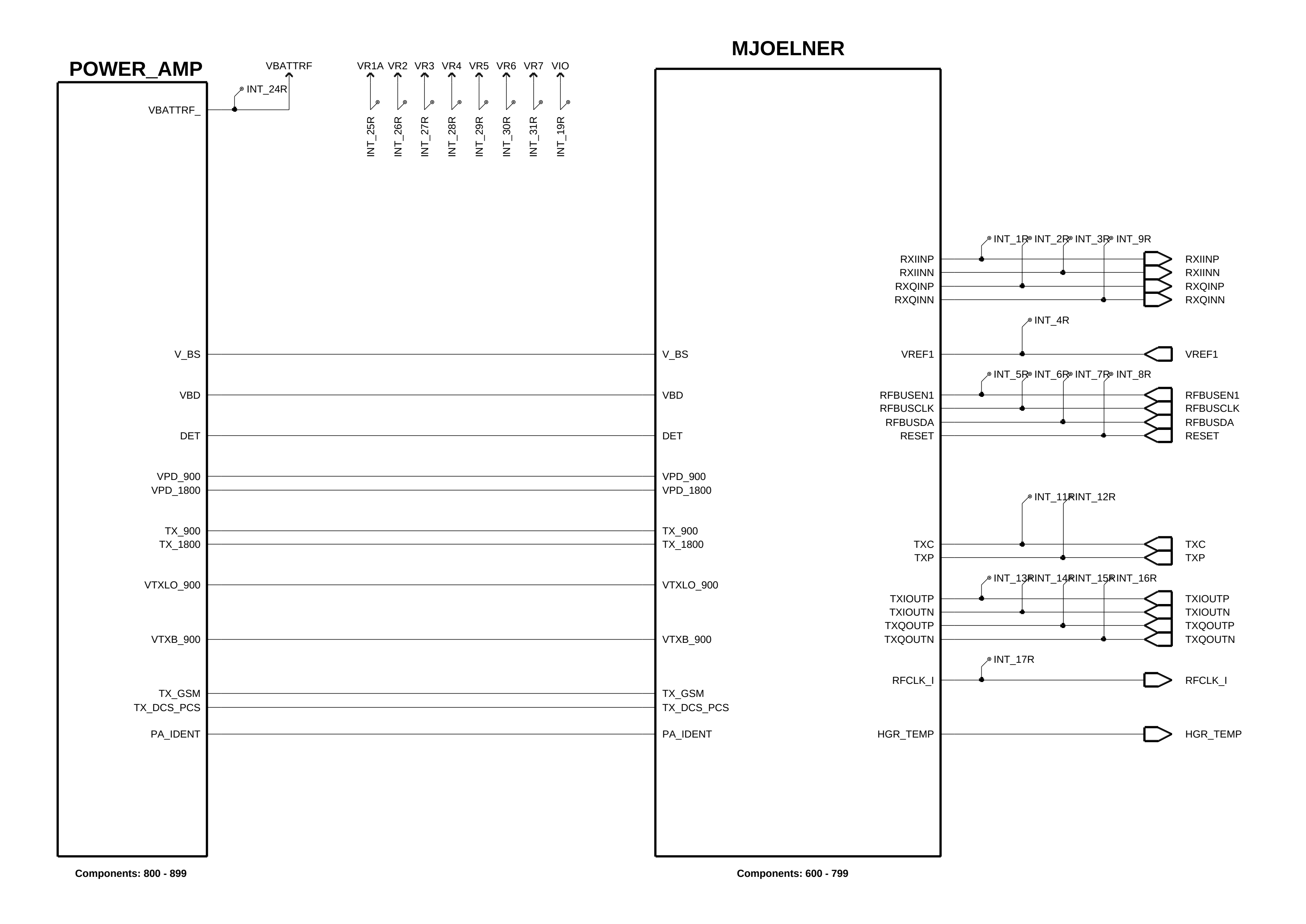




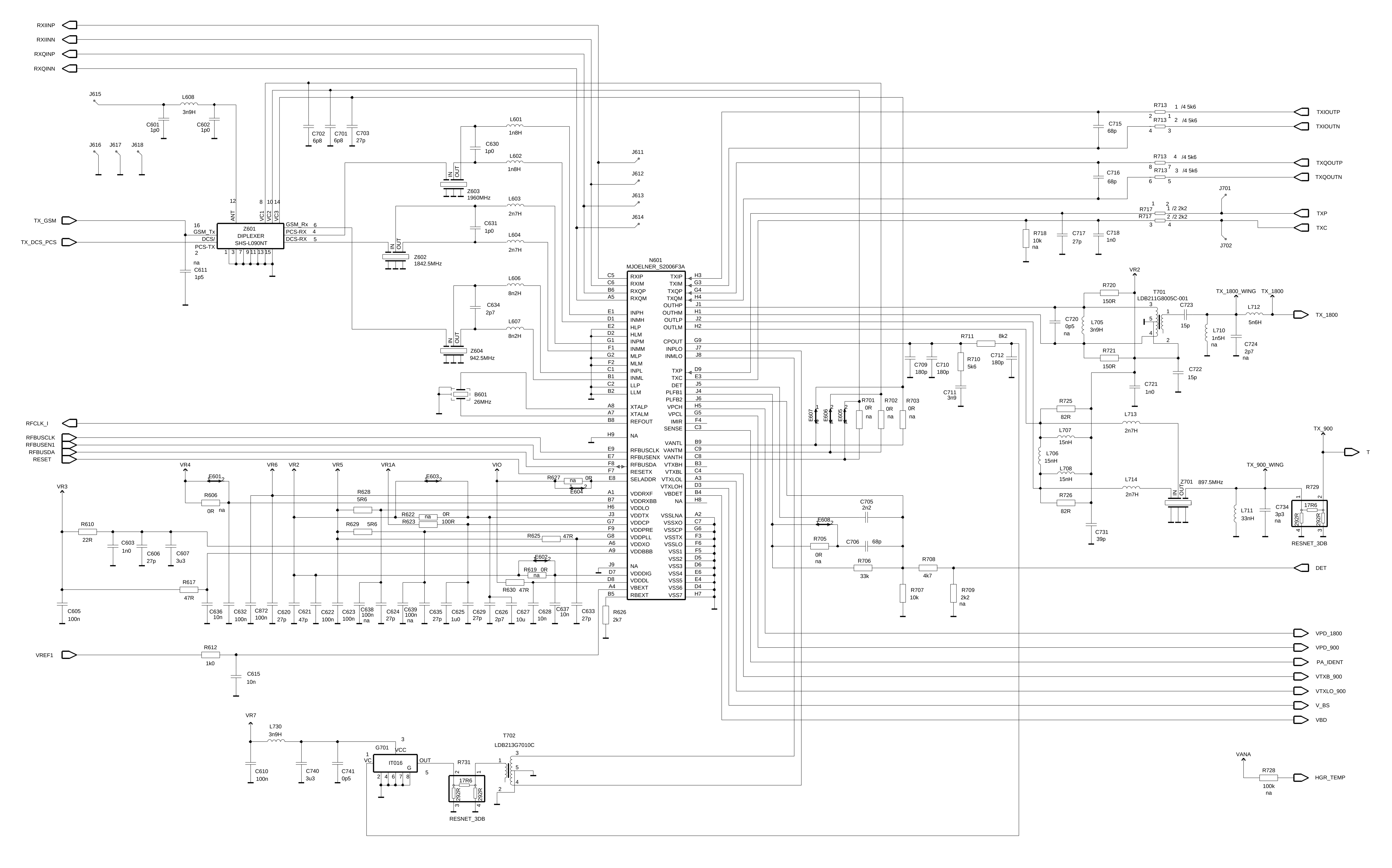
Title: 5 pin Production Test Pattern



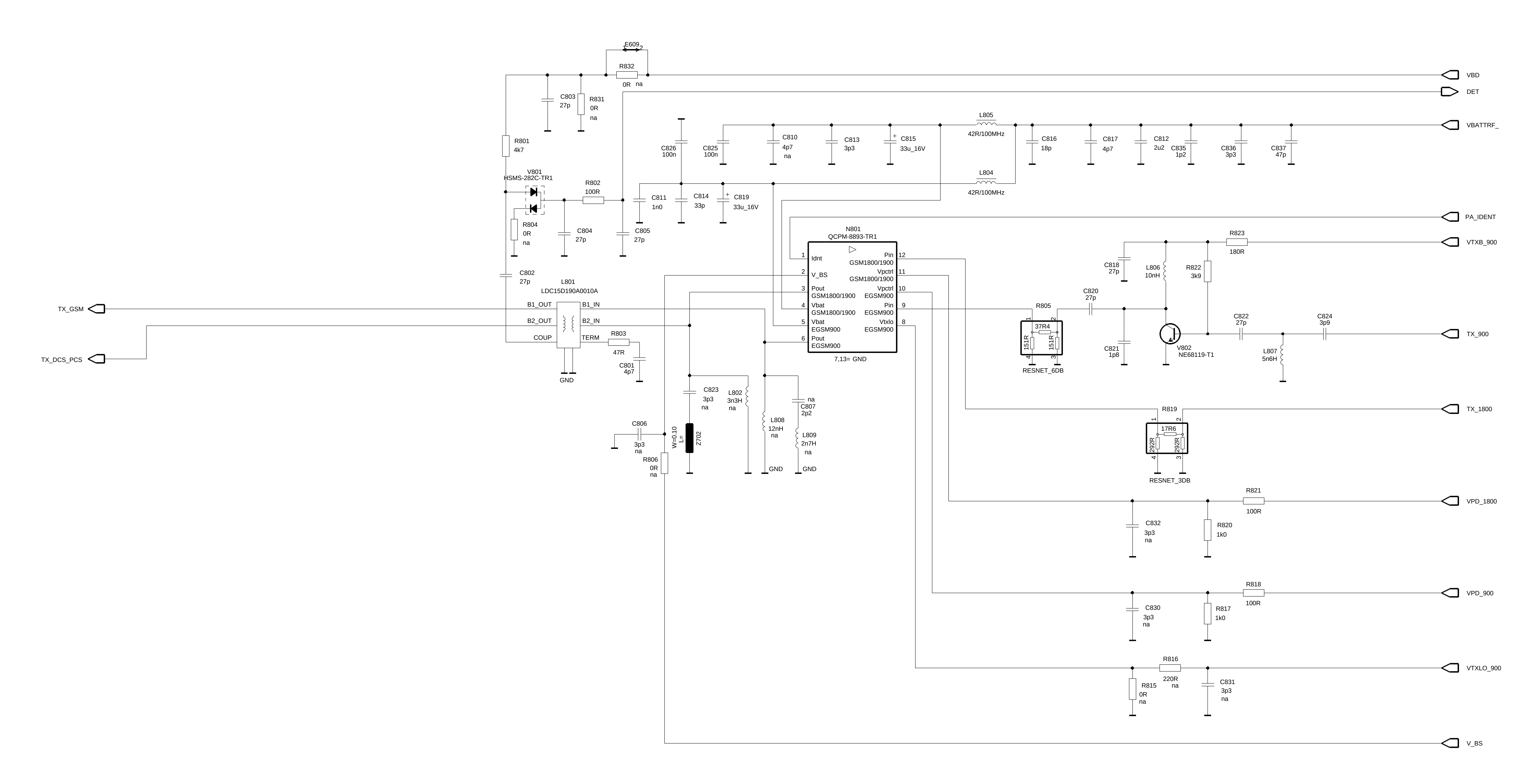
Title: RF top sheet schematic



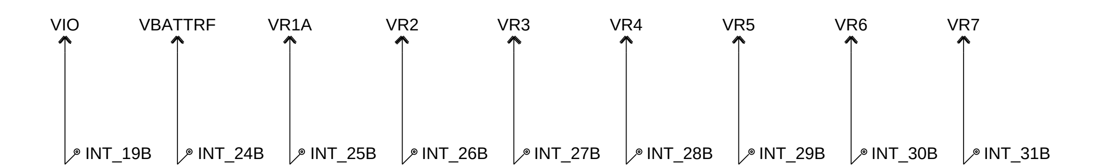
Title: Mjoelner

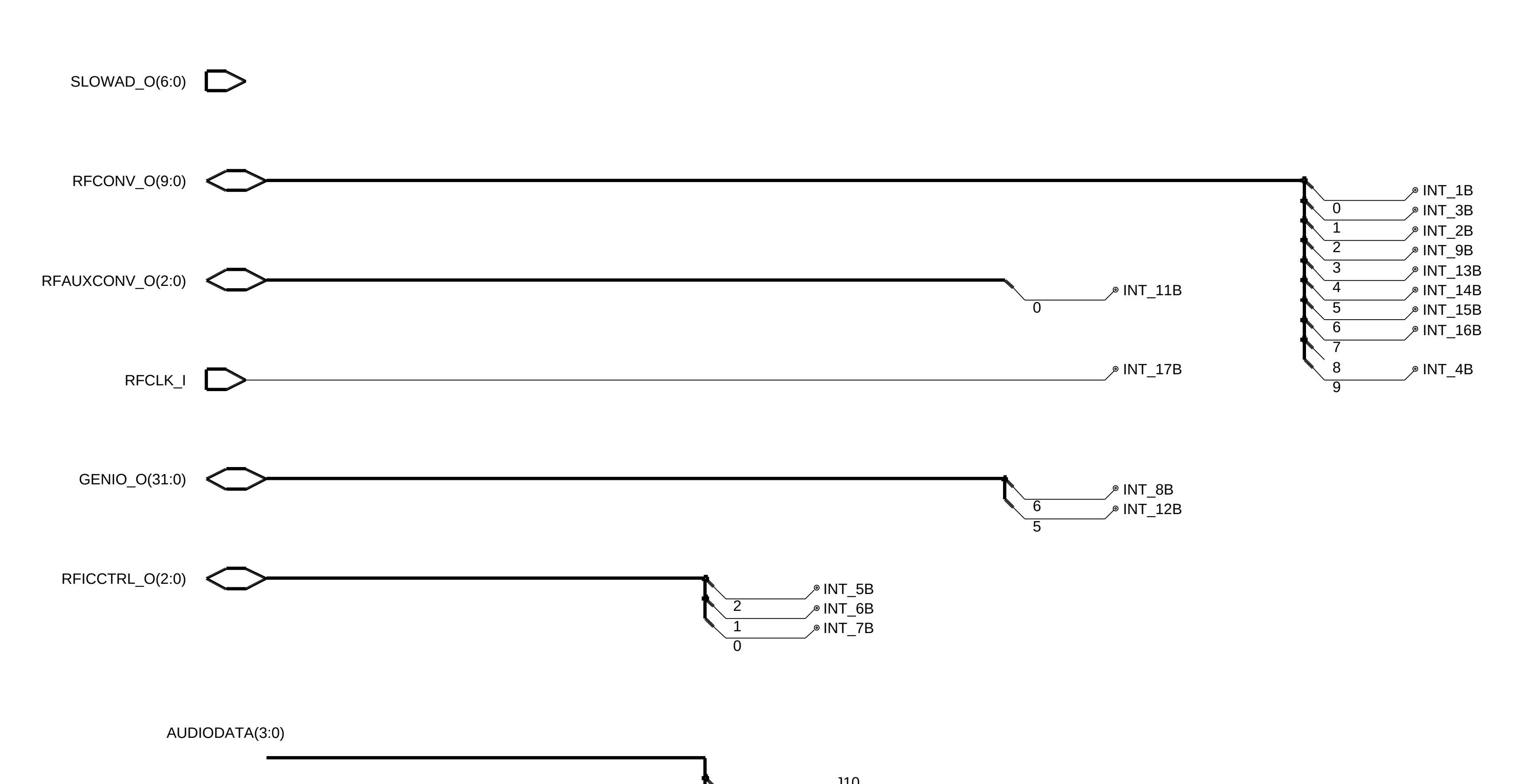


Title: Power amplifier

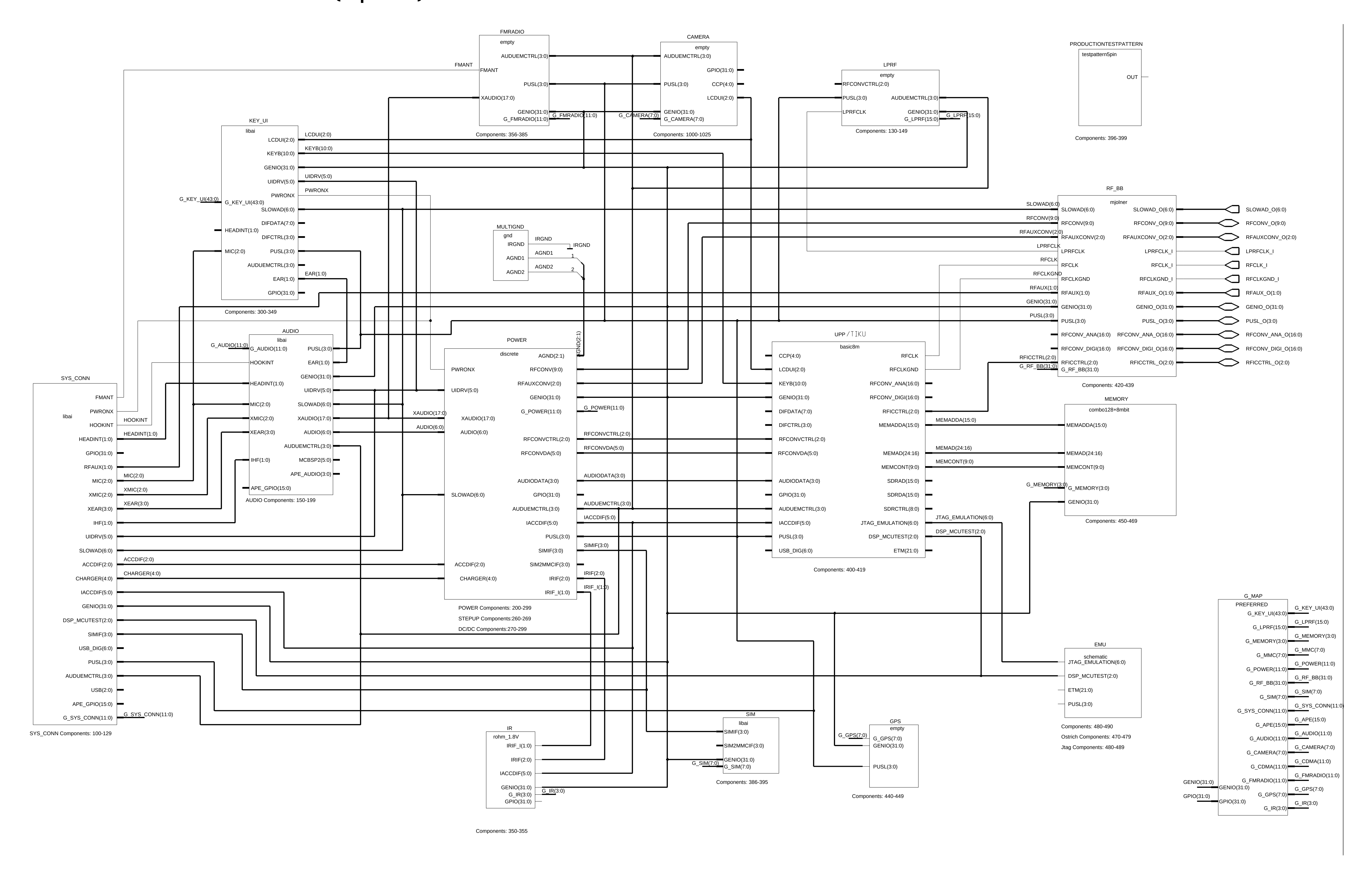


Title: BB RF interface components

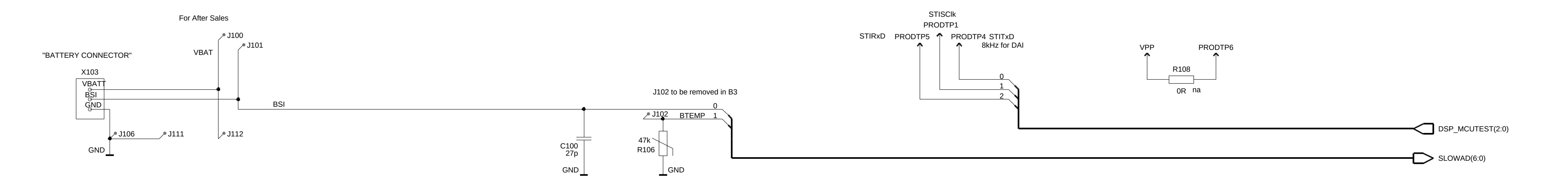


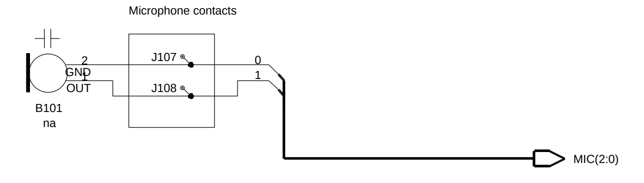


Title: DCT4 common BB Schematic (top level)

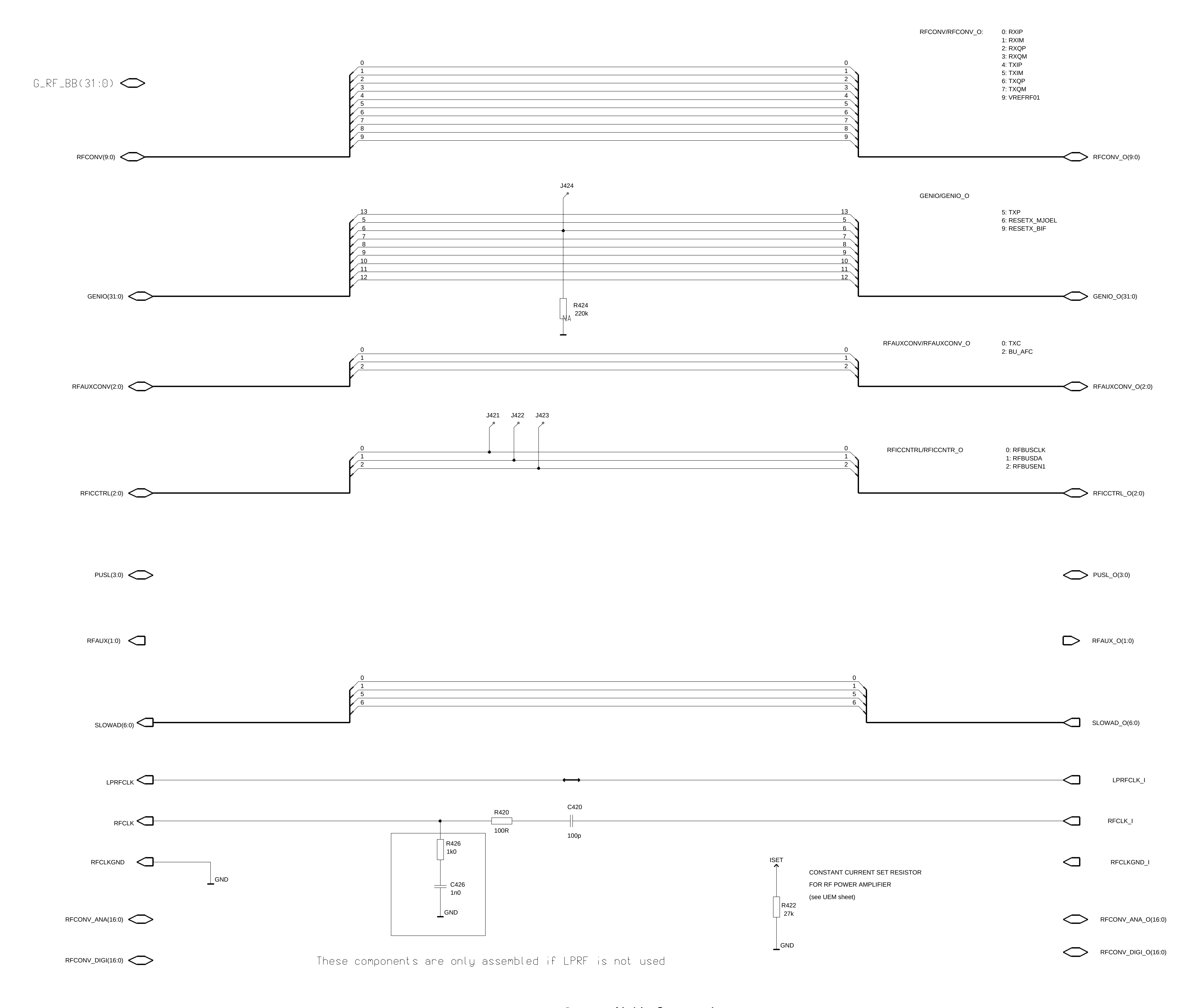


Title: RH-4 System connector

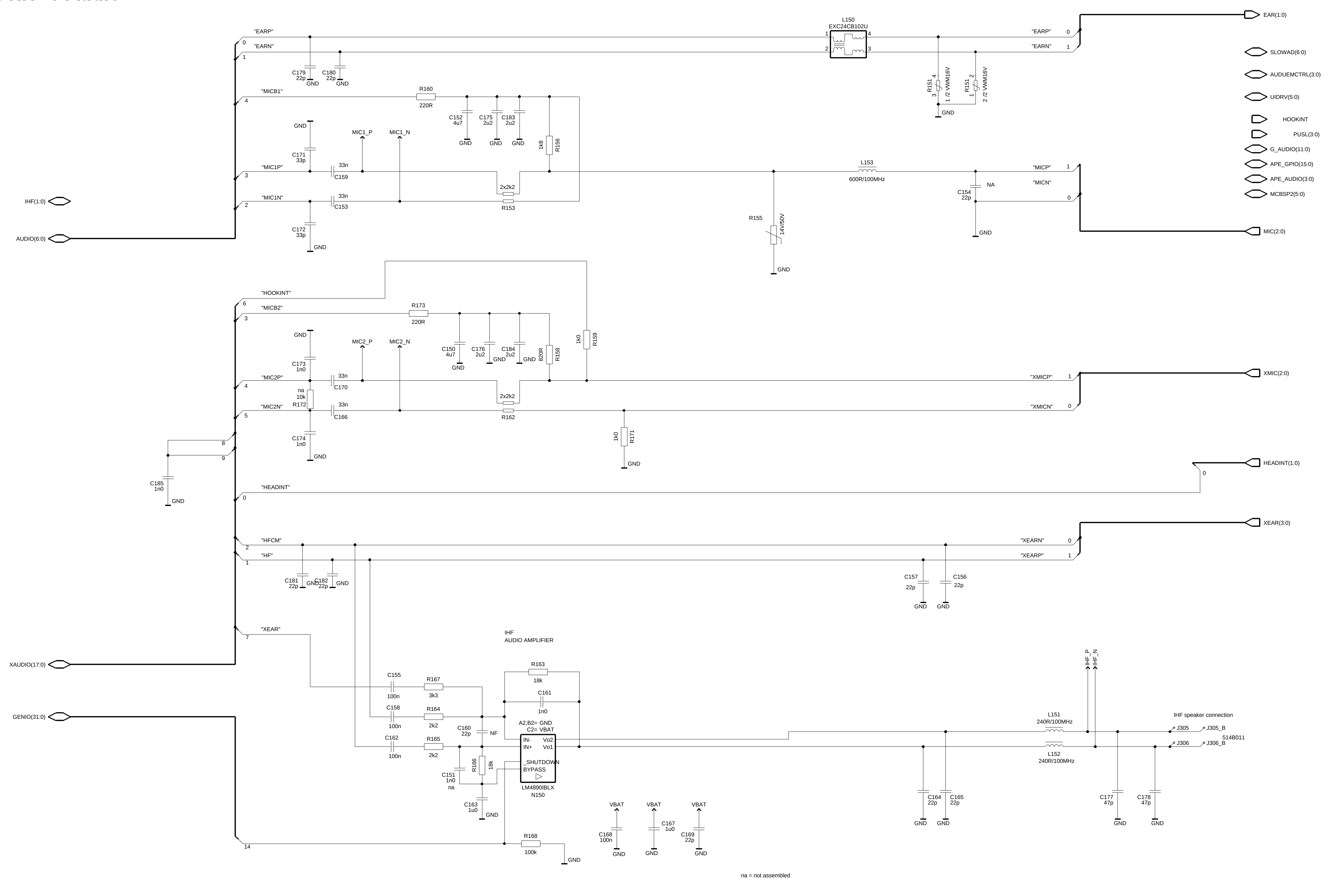




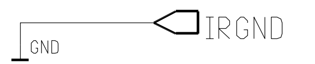
Title: GSM RF BB interface



Title: RH-4 Audio



Title: MultiGND symbol bypass



GND AGND1

GND AGND2

Title: GENIO and GPIO connection block

GENIO(31:0)

GPIO(31:0)

G_APE(15:0)

G_AUDIO(11:0)

G_CAMERA(7:0)

G_CDMA(11:0)

G_FMRADIO(11:0)

G_GPS(7:0)

G_IR(3:0)

G_KEY_UI(43:0)

G_LPRF(15:0)

G_MEMORY(3:0)

G_MMC(7:0)

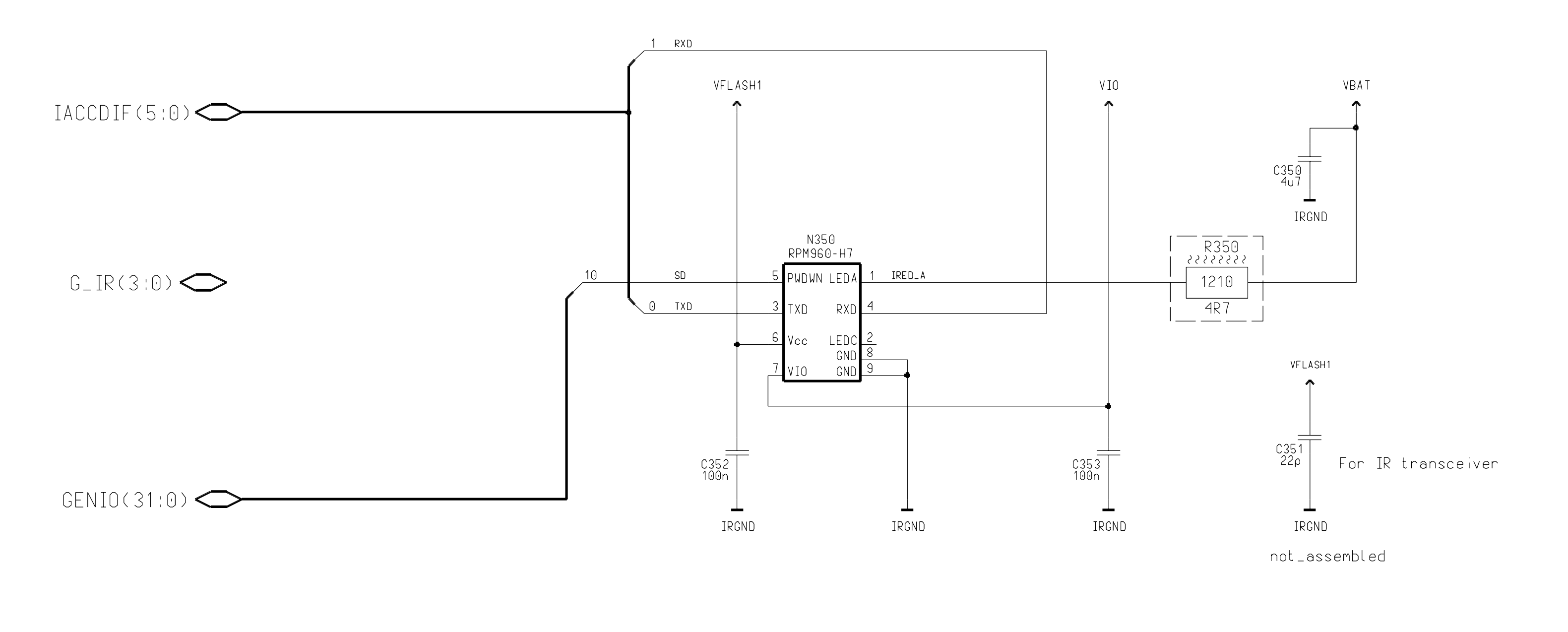
G_POWER(11:0)

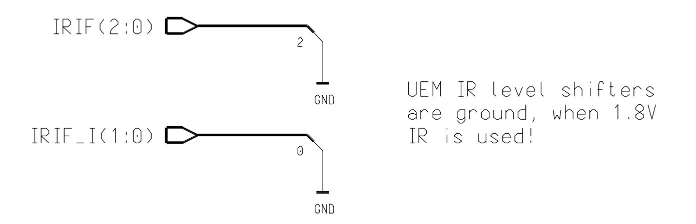
G_RF_BB(31:0)

G_SIM(7:0)

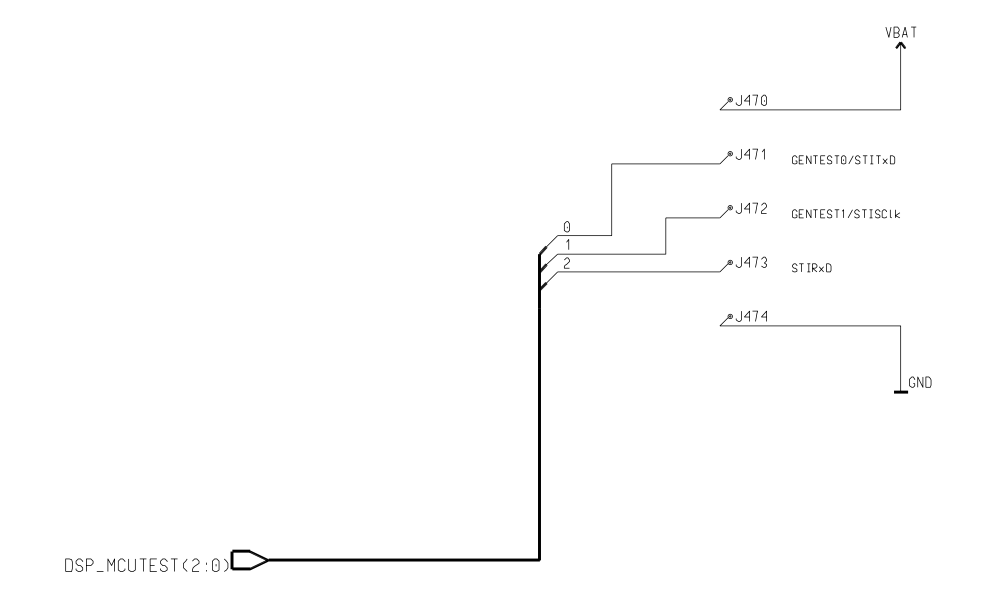
G_SYS_CONN(11:0)

Title: Rohm IR module 1.8V

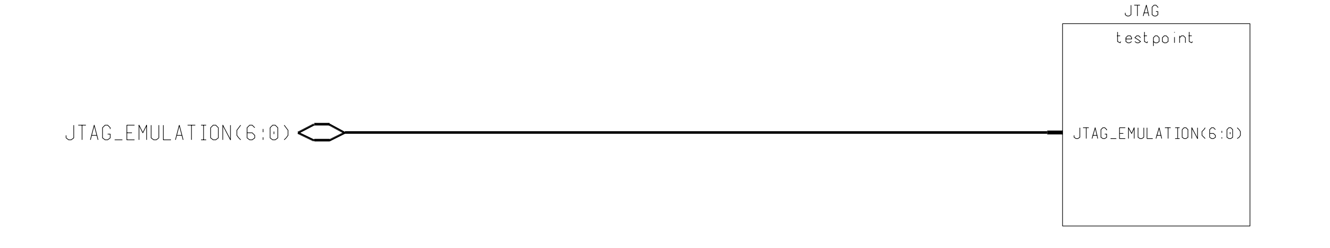




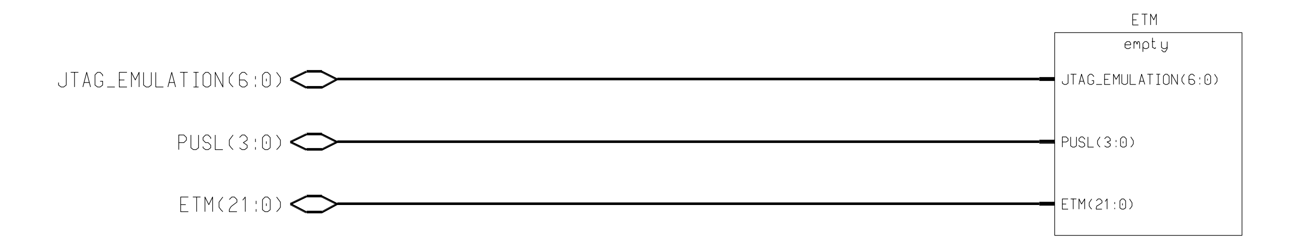
Title: Testpoints based Ostrich interface



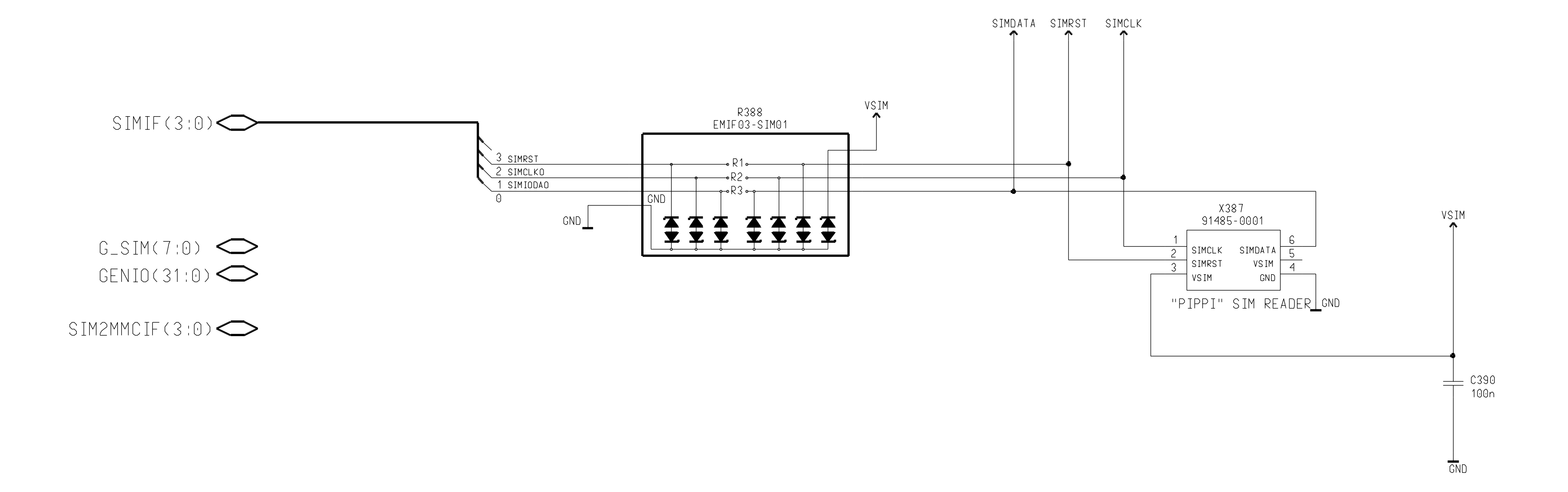
Title: Test and emulator interface



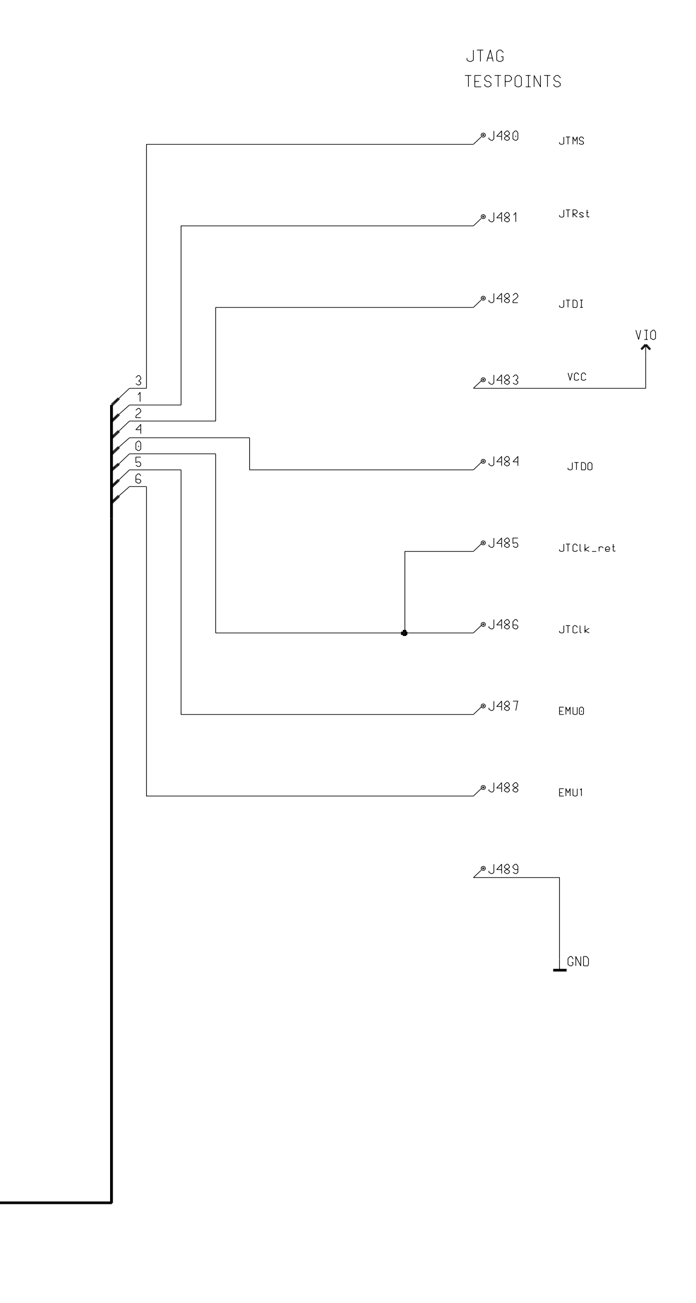




Title: SIM reader



Title: Testpoints for JTAG emulator



JTAG_EMULATION(6:0)

Title: DC/DC convertor

VCORE_LIN

VCORE

GENIO(31:0)

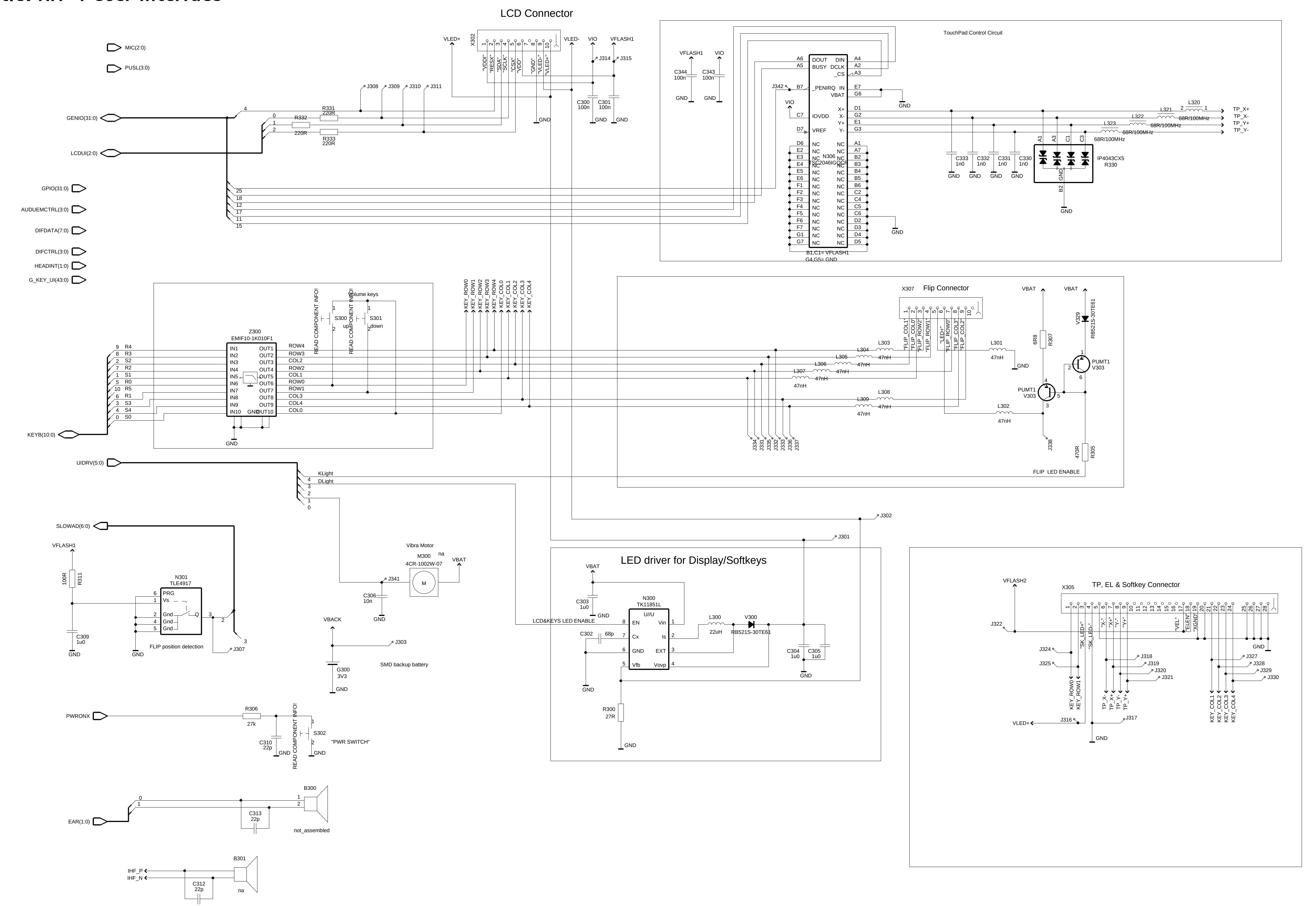
G_POWER(11:0)

UEMRSTX

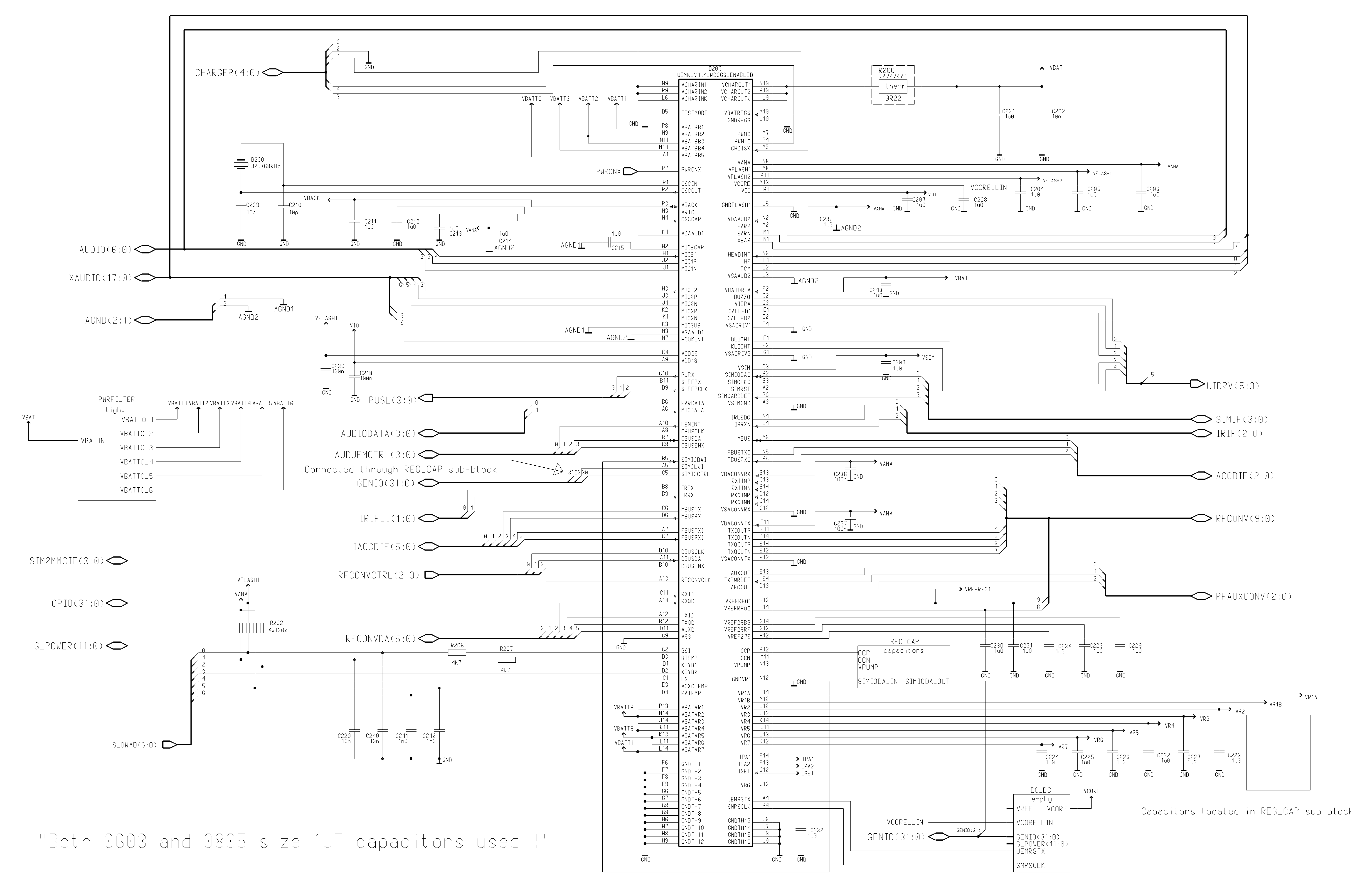
SMPSCLK

VREF

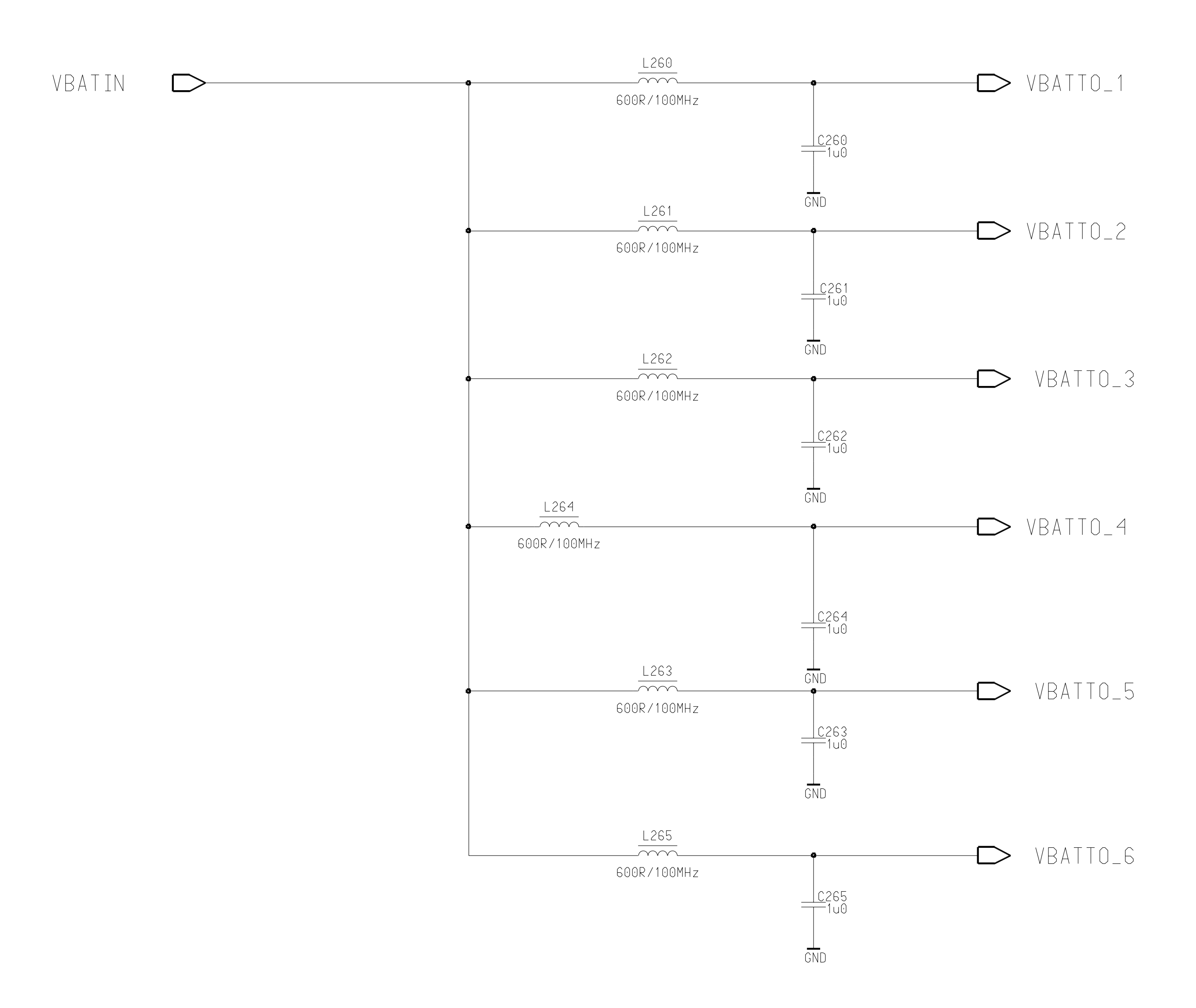
Title: RH-4 User interface



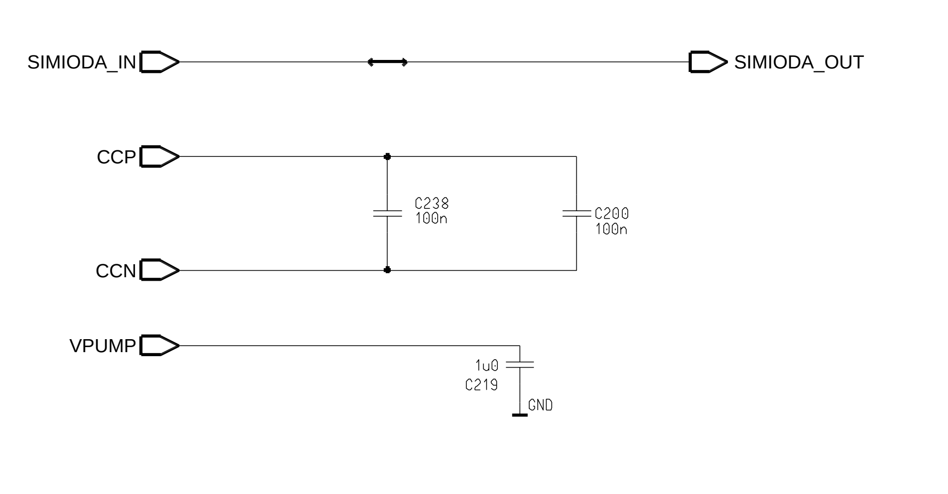
Title: Discrete power management



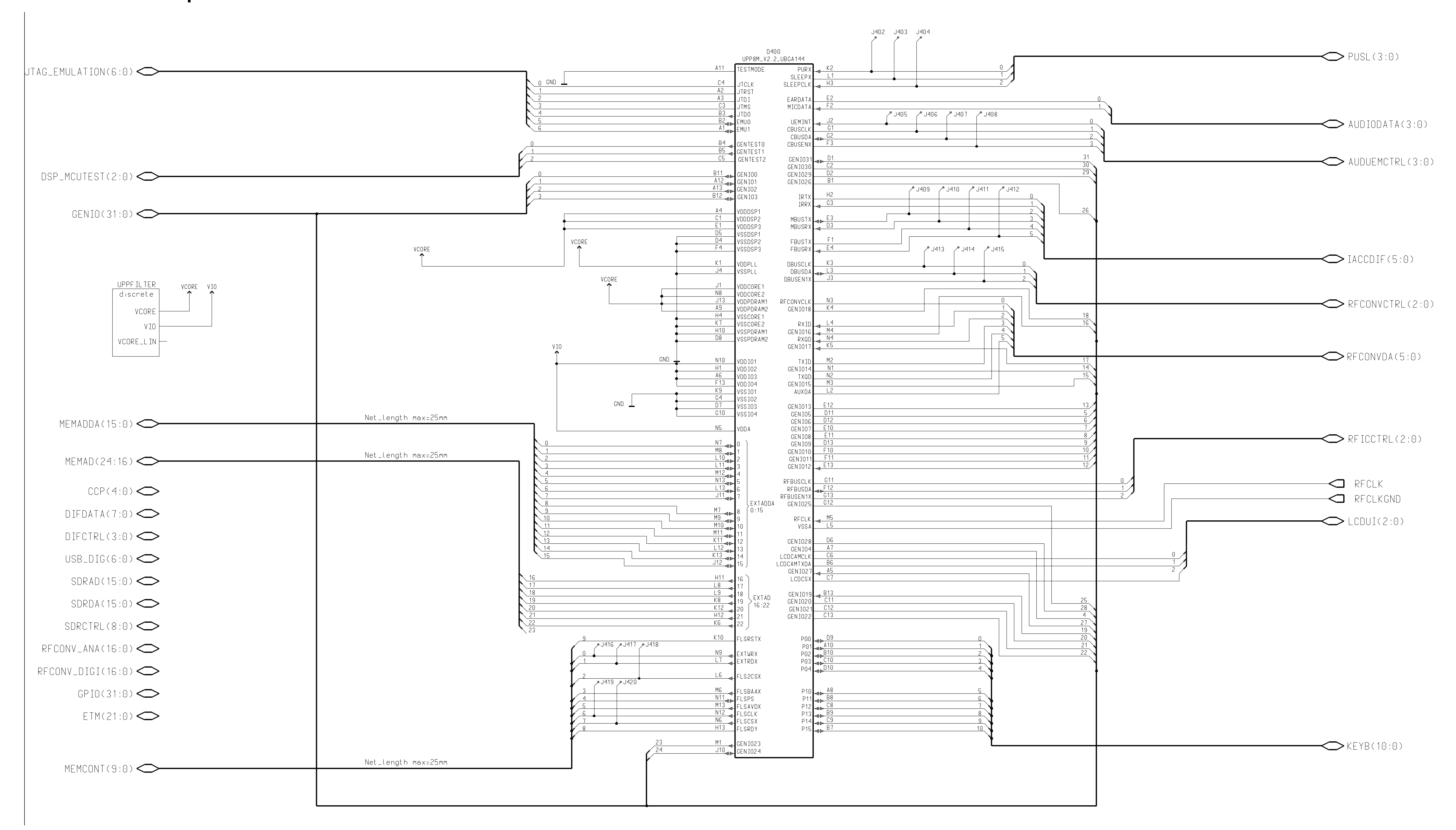
Title: Light filtering



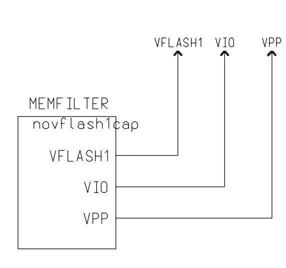
Title: Old power discrete users



Title: UPP 8M implementation



Title: Combo memory 128 +8 Mbit



MEMEXTENSION
empty
MEMADDA(15:0)
MEMAD(24:16)
MEMCONT(9:0)
GENIO(31:0)
G_MEMORY(3:0)
FLS2CSX

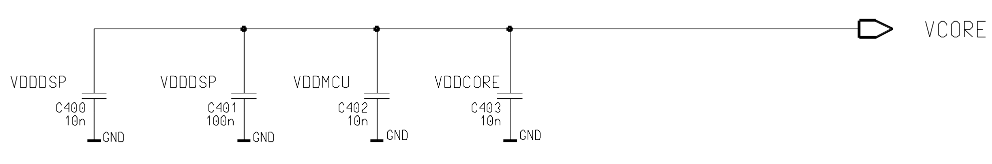
MEMWING
empty
GENIO(31:0)
G_MEMORY(3:0)
MEMAD(24:16)
MEMADDA(15:0) FLS2CSX
MEMCONT(9:0) FLSCSX

GENIO(31:0)
MEMAD(24:16)
MEMADDA(15:0)
MEMCONT(9:0)

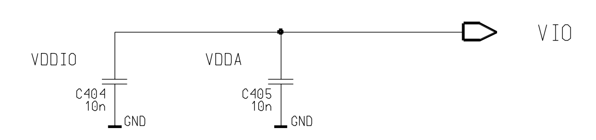
D450
NMP_DCT4_128MNOR_8MSRAM
FLASHM 8Mx16
SRAM 512kx16
MEMAD(16) B2 16
MEMAD(17) A9
MEMAD(18) B8 A
MEMAD(19) A8
MEMAD(20) B3 20
FLASH/SRAM
MEMAD(21) A2 A21/_LB
MEMAD(22) A10 A22/_UB
B7 _WP/_CS
FLASH
MEMCONT(6) A4 CLK RDY A1
MEMCONT(9) B6 _RESET
B9 _CEF
NC 1 E451
NC 2 E452
NC 3 E453
COMMON NC 4 E454
MEMCONT(5) B4 _AVD NC 5 E455
MEMCONT(0) A6 _WE NC 6 E456
MEMCONT(1) C10 _OE NC 7 E457
MEMCONT(4) B5 PS NC 8 E458
ADDRESS/DATA I/O
0 D10
1 D9
2 C7
3 C6
4 D5
5 D4
6 C3
7 C2
8 C9
9 C8
10 D7
11 D6
12 C5
13 C4
14 D2
15 D1
VPP PRODTP6
MEMCONT(3) R450 4k7 E450
MEMCONT(8)
A5,B1,D8=VIO
A7=VPP
A3,B10,C1,D3=GND

GENIO(31:0) 23
MEMAD(24:16)
MEMCONT(9:0)
MEMADDA(15:0)
G_MEMORY(3:0)

Title: Discrete decoupling capacitors for UPP



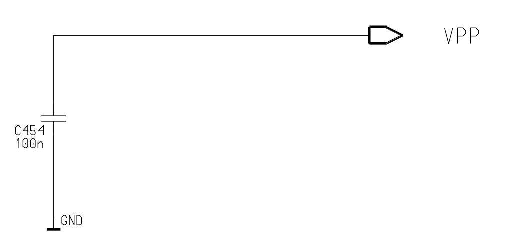
VCORE_LIN



Title: Discrete capacitors for memory without VFlash 1



VFLASH1



Title: Empty wing sheet

